	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	39314	gate adj1 oxide$1	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 16:48
2	BRS	L2	11	silicon adj1 nitride near5 (third near5 silicon adj1 oxide)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 16:49
3	BRS	L3	46	1 and 2	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 16:49
4	BRS	L4	44	3 and transistor	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 16:50
5	BRS	L5	131	(silicon adj1 nitride) near5 (third near5 silicon adj1 oxide	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 16:51

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	39	1 and 5	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_T B	[illegible]
7	BRS	L7	70	[illegible] adj1 nitride, near5 (third near5 silicon adj1 dioxide)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/03 17:31
[illegible]	BRS	[illegible]	[illegible]	and thickness	USPAT; US-PGP UB; EPO; [illegible] DERWEN T; IBM_TD B	[illegible]
9	BRS	L9	40	8 and transistor	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/03 17:18
[illegible]	BRS	[illegible]	[illegible]	[illegible] near5 (third near5 dielectric)	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	[illegible]

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L11	111	10 and thickness	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 17:31
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
13	BRS	L13	262	(silicon adj1 nitride) near5 (third near5 insulating)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2002/04/03 17:49
[illegible]	BRS	[illegible]	[illegible]	[illegible]	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]
15	BRS	L16	4	15 and second adj1 thickness	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	[illegible]

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L17	6	15 and first adj1 thickness	USPAT; US-PGP UB; EPO; JPO; DERWEN T; IBM_TD B	2002/04/03 17:53
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

	U	1	Document ID	Title	Current OR
	☐	☐	[illegible]	SEMICONDUCTOR DEVICE AND [illegible]	[illegible]
	☒	☐	US [illegible]	[illegible] integrated circuit with an insulant structure having reduced permittivity	[illegible]
3	☐	☐	US 6020644 A	Semiconductor memory device having bit lines and signal wiring layers different in thickness and process of fabricating thereof	257/775
4	☐	☐	US [illegible] A	Semiconductor device and [illegible]	[illegible]
5	☐	☐	US [illegible] A	Cross-point eeprom memory array	[illegible]
6	☐	☐	US 5384731 A	SRAM memory structure and manufacturing method thereof	365/182